

# On nano architectural challenges and some potential solutions

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In the nanoelectronic era, the growing complexity (in number of devices) of integrated circuits (ICs) turns acute problems (e.g., power and reliability) into great challenges, while communication problems (increased delays) will lead to network-on-chip, forcing (partly) asynchronous solutions. Out of the many nanoelectronic challenges, we shall focus here only on those where an architectural approach could make a difference. As an example, one well-known challenge is the ever-increasing dissipated power (and heat). This should be approached starting from the low level (nano devices), and going all the way up to system level. Reconfigurability could certainly help in reducing power. Another challenge is communication, which could be (partly) solved by using optical interconnects. It is expected that a globally asynchronous locally synchronous (GALS) type of communication would be an easier solution for the near future, as not requiring optical wave-guides. Still, one could envisage a combination, like a globally optical locally electrical (GOLE) solution.

A list of nanoelectronic challenges where architecture can make a difference should include: power (reduction, delivery, distribution); heat (reduction, removal, dealing with hot spots); interconnects (reduce length/delay, reduce number); testability/verification (reducing associated costs); reliability (economical redundancy factors, reconfiguration, adaptive); communication (low-power, non-flooding, reliable); hybrid integration (mixed design, interfacing); logic and coding (non-Boolean, error correction, spikes); algorithms (stochastic/probabilistic); and design complexity (reduce associated cost by reuse). Going thoroughly over these challenges, and over the links amongst them, we will rank them with respect to their overall importance. The motivation for such an exercise is to identify clearly the challenge(s) on which to focus more research effort. For doing this, we will assign a percentage to each of the challenges, reflecting its relative importance, while a *correlation matrix* will be used to capture *second order effects*, namely the ways one challenge is affecting the other challenges. Let us take connectivity as an example. Reducing connectivity should reduce power/heat, having a positive influence. On the other side, the overall length of the wires should be increased when considering any kind of redundancy (needed for increasing reliability), therefore reducing connectivity could have a negative influence on reliability.

Potential solutions will be presented and classified in three groups: near term solutions, medium term solutions, and long range ones. Near term solutions include: massively parallel, modular (cells, blocks); regular (grid processing, cellular arrays); locally connected (near-neighbor connections, crossbar); higher functionality (multiple valued logic, threshold logic); reconfigurable (self-mapping). Medium term solutions: asynchronous (including GALS); fault-tolerant (noise immune, rad-hard by design, redundant, self-testing, self-correcting); defect-tolerant (reconfigurable); redundant; adaptive (self-adaptive, self-organizing, evolvable); bio-inspired (complex functions, self-organizing, self-healing); nanophotonic (optical communication, GOLE); nanofluidic; 3D interconnects; probabilistic (algorithms, encoding, communication). Long term solutions: molecular, quantum; quantum-dot cellular automata; adiabatic/reversible; bio-compatible.

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