

Semi-Vertical SWNT FETs: Steps towards Verticality and Manufacturability

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Single-walled carbon nanotubes (SWNTs) are a potential channel material for the next generation field-effect transistors (FETs). With properties such as ballistic transport and high thermal conductivity, SWNT FETs have the ability to outperform Si MOSFETs [1]. To date, all reported SWNT FETs have been created in a planar geometry, with the SWNT horizontal to the supporting substrate. Planar SWNT FETs have provided an important platform for exploring device properties. Using this configuration, a variety of contact/dielectric materials and other parameters have been studied, demonstrating the outstanding capabilities of the SWNT devices. However, the planar geometry processes have not been able to address the impending issue of large-scale device fabrication.

To fabricate SWNT FETs on the scale of an integrated circuit, two significant obstacles remain: 1) synthesis of vertical SWNTs in predefined locations, and 2) control over the chirality of the SWNTs. While the latter of these two obstacles has not yet been solved, synthesis of vertical SWNTs in predefined locations has been reported recently [2]. By embedding a Fe catalyst into porous anodic alumina (PAA), individual SWNTs grow vertically within the pore channels. Further work has led to Pd nanowire contacts to the bottom of the SWNTs within the pores [3,4], producing vertical channels approximately 20 nm in diameter and containing a vertical SWNT emerging from a vertical Pd nanowire. In order to examine the Pd nanowire contact to the SWNTs, semi-vertical SWNT FETs are fabricated by patterning the PAA structure next to silicon dioxide as shown in Figure 1. Atomic layer deposition (ALD) is used to form an alumina gate dielectric, and gate and drain contacts are formed using optical lithography.

The Pd nanowire contact of the semi-vertical SWNT FETs is studied in comparison to a traditional planar metal contact. Using the same structure, FETs are

created with top-planar contacts for both the source and drain, which supplies a comparison to the semi-vertical devices. Previous work with Pd top-contacted SWNTs has shown that transport occurs at the edge of the Pd electrode while the remainder of the Pd-covered SWNT is electrically turned off [5]. In the case of the present vertical Pd nanowire contact, evidence suggests that the Pd surrounds the SWNT annularly, thus providing the maximum transport area between the SWNT and Pd contact.

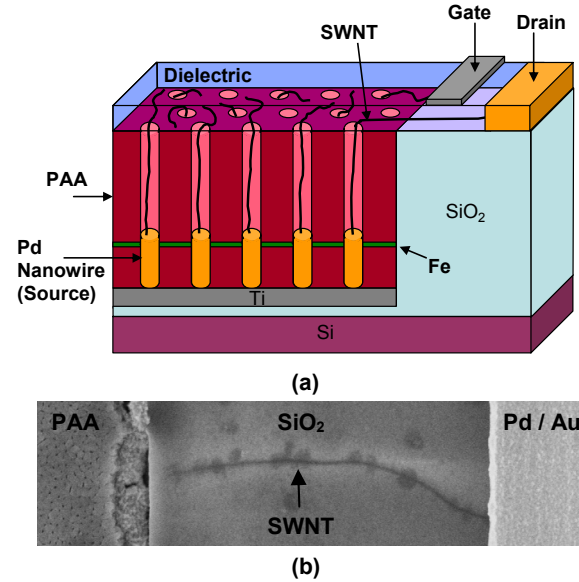


Fig. 1 (a) Schematic of semi-vertical SWNT FET showing the PAA/SWNTs (with vertical Pd nanowire contacts) patterned next to SiO₂ and a SWNT extending onto the oxide surface where the device is gated and top-contacted. (b) FESEM top-view image of SWNT emerging from PAA onto the oxide and beneath a top Pd

In order to begin solving the large-scale integration problem, SWNT FETs should be created with total verticality. With evidence of the advantageous properties of the vertical Pd nanowire contact, the PAA/SWNT structure is a suitable platform upon which such vertical SWNT FETs can be fabricated. Application of an annular gate dielectric, combined with further processing, will create completely vertical devices with the potential of achieving a density equal to that of the PAA template ($\sim 10^{10}$ pores/cm²). By including a few pores of SWNTs per FET, the current-carrying ability can be many times that of Si MOSFETs while still maintaining a nanoscale footprint.

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