Innovating SOI Memory Devices Based on Floating-Body Effects

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The scaling requirements of conventional memory devices lead to recent developments of capacitor-less DRAM in SOI technology such as Z-RAM (Zero RAM), TTRAM (Twin-Transistors RAM), and more recently MSDRAM [1,2,3,4]. In this paper, the devices architecture, operating principles and memory performances are critically reviewed.

In SOI floating-body memories, the body capacitance is used instead of the standard DRAM capacitor. The memory storage mechanism is based on the threshold voltage shift produced by majority carriers accumulation (or depletion) in the floating body [5]. Since there is no body contact, equilibrium is reached after a relatively 'long' period of time which renders SOI memories rather attractive in terms of retention and refresh time. The writing (*i.e.*, body charging) of these memories makes use of impact ionization and/or band-to-band tunneling (GIDL). Main advantages of capacitor-less memories, compared to conventional DRAM [6,7], are the cell size reduction and non-destructive reading.

The Z-RAM uses a single SOI transistor and is suitable for sub-100-nm technology [8]. Its cell size is smaller than that of embedded DRAM and about one-fifth of a six-transistor SRAM area. With the trench and stacked capacitors of conventional embedded DRAM becoming more difficult to build, Z-RAMs look cheaper and require few additional mask layers. In addition, a Z-RAM demonstrates fast write times. Nevertheless, several critical issues are noted: (i) the need for complex array control due to various internal voltages, (ii) the 1T gain cell may be insufficient for high-speed operation, (iii) the difficulty to control the reference voltage since the floating body is not tied to a fixed voltage (the stored charge can easily fluctuate), (iv) the relatively low current level difference between "1" and "0" states, (v) the significant power consumption during programming "1" and reading "0".

The TTRAM which also uses floating-body charging needs two SOI transistors. Although its cell size is twice as large as for Z-RAM, the area gain stays very attractive by comparison with conventional embedded DRAM. Z-RAM and TTRAM provide similar advantages: fast write time, no additional mask, non destructive read, and scalability. The noticeable difference resides in the simple array control which allows TTRAM achieving high-speed operation.

The basic mechanism of the MSDRAM (one-transistor capacitor-less RAM) lies in the Meta-Stable Dip (MSD) effect [9]. MSD uses the double-gate action in regular SOI MOSFETs, namely the coupling between front and back interfaces, and gives rise to a hysteresis in $I_D(V_G)$ curves and a dip in transconductance. The occurrence of the front accumulation layer disables the front-back interface coupling leading to inverted back interface ('1' state). Reciprocally, '0' state corresponds to an absence of the front accumulation layer: the front-back interface coupling is now enabled which causes depletion at the back interface, hence suppression of the drain current. Since interface coupling is the key effect, the MSDRAM is appropriate for double-gate structures enabling a reasonable low back-gate biasing.

The novel MSDRAM is simple to fabricate, program and read. It exhibits a very long retention time (10 s range) and a relatively short programming time (1 μs range). The drain bias (100 mV range) and the read currents (nA to μA range) are suitable for low-power applications. In terms of scaling, measurements indicate that channel length reduction is beneficial: the programming time is considerably reduced, whereas the '0' state retention time remains longer than 25 s. Systematic experimental and simulated data will be presented to demonstrate the attractiveness of MSDRAMs.

Finally, we will discuss the compatibility of the capacitor-less DRAMs with advanced technologies: from PD and FD SOI to FinFETs, MUGFETs [10], and double-gate devices [11].

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