Designing Nanotechnology Circuits – The Interconnect Problem

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As progress along the ITRS road map continues, physical and electromagnetic limitations make scaling of silicon FETs increasingly difficult. One solution is to replace FETs by completely new structures such as nanoscale molecular, biological or quantum devices. Before considering this changeover, an interconnect technology must be developed that is suitable for these new device concepts. To connect ultra-small devices, interconnects must be less than 10 nanometers (nm) in diameter. However, they still must be easy to fabricate, have low resistance, high maximum current carrying capacity and be isolated by low-k dielectric materials for applications in ultra-high density nanotechnology circuits. As the sizes of the active devices approach the nanometer dimensions, the wires that connect them must also be scaled down. Today, several IC manufacturers are in the process of commercializing 100 nm CMOS-based IC technologies and the research & development work for the 70 and 50 nm devices is well underway. Successful IC development below these feature sizes faces the fundamental challenges imposed by the basic lays of quantum physics. The surface scattering from the boundaries of ultra-narrow conductors as well as the grain boundary scattering would inhibit electronic conduction in the wires to an unacceptable level.

Nanotechnology circuits with devices on the sub 100 nm scale will require interconnects with sizes from 50 nm down to molecular and atomic dimensions. If metallic conducting lines such as copper are used for the interconnects then the miniaturization process will result in rise in the copper resistivity because the dimensions of the conducting lines will be of the same order of magnitude as the mean free path of electrons which is 39.3 nm in copper at room temperature. This rise in resistivity may dramatically slow the circuit's functioning and as a result jeopardize the ability to improve the circuit speed expected from miniaturization. Electromigration which is the result of momentum transfer from the electrons moving under the applied electric field to the ions making up the lattice structure of the interconnect material imposes another serious problem. Continuing miniaturization of the thin-film metallic interconnects results in increasingly high current densities leading to the open- and/or short-circuit electrical failures of interconnects in a relatively short time. The higher the temperature of operation, higher the electromigration-induced failure of the metallic interconnects is.

Clearly, interconnects will play a crucial role in the development of the nanoscale integrated circuits and that, in addition to the development of the various nano devices, interconnects that will be used to connect these devices deserve a very special attention. In this paper, the various potential interconnect technologies suitable for nanoscale integrated circuits including modified metallic interconnect designs, nanowires, carbon nanotubes and quantum cell based wireless interconnects will be discussed. In addition, the importance of the interconnect parasitics such as capacitances & inductances and performance parameters such as propagation delays, crosstalk and current carrying capacities for almost electromigration-free operation for the various potential interconnect technologies in the nanoscale regime will be highlighted.

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