Structure-Reliability Relation in Advanced Transistor Gate Stacks

Gennadi Bersuker*, Byoung Hun Lee,Raj Jammy

SEMATECH, 2706 Montopolis Dr., Austin, TX 78741, USA

After many years of research on conventional SiO2 gate dielectrics, the mechanisms governing dielectric degradation under various use conditions remain a topic of active investigation. In advanced gate stacks, reliability assessments are further complicated by the introduction of high-k dielectrics and metal gate electrodes, which gives rise to a number of specific issues. On an atomic level, a common electronic feature of high-k materials is the presence of d-shell states, which make their structural properties drastically different from those of conventional SiO2 gate dielectrics.One of the consequences of the d-electron bonding in high-k dielectrics is a relatively high density of as-grown defects, which have been shown seconds)µto contribute to reversible electron trapping with short (and long (seconds) characteristic trapping times. This phenomenon questions the traditional reliability concept, which assumes that the stress time dependency of electrical parameters is indicative of time-dependent degradation of the dielectric. It has been shown that a high density of pre-existing defects may lead to a parameter time-dependency without defect generation.

Another important feature of high-k gate stacks is that they are usually represented by a multi-layer structure. In particular, in Hf-based dielectrics, the stack includes a high-k dielectric and a thin interfacial SiO2 layer (IL), which is grown either intentionally or unintentionally on the Si surface. Each of these layers, in turn, is rather non-uniform since they are affected by interlayer interaction (influence of high-k films on the structure and composition of IL, metal gates on high-k films, etc). Stress-induced changes in the transistor parameters may originate from defect generation in both the high-k and SiO2 layers, in which degradation is expected to be controlled by different mechanisms. A failure to separate contributions from the high-k and IL would lead to erroneous projection of reliability.

Due to these features of high-k gate stacks, an assessment of their reliability calls for an approach that combines electrical, physical, and material modeling methods. In particular, applying pulsed Id-Vg measurements in a range of nanoseconds and variable frequency charge pumping (which can delineate fast trapping contributions and trapped charge locations, respectively) along with profiling of the stack composition (by high resolution EELS, XPS, ESR, etc.) and ab initio modeling of the dielectric structure allows electrically active defects to be identified and physical models for device life-time evaluation to be developed.

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*Corresponding Author.

Email Address. gennadi.bersuker@sematech.org (Gennadi Bersuker)