Silicon-On-Insulator Nanopore Arrays for Ion Channel Sensors

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Ion channels are transmembrane proteins that facilitate the diffusion of ions and small molecules across the phospholipid bilayer membrane of cells. These proteins possess the capability to open and close due to various stimuli, including: voltage, temperature, pressure and ligand binding events. This ability defines the proteins as very small natural sensing elements [1]. The study of ion channels can take place either in situ using a technique known as patch-clamping developed by Neher and Sackmann [2] or by bilayer reconstitution techniques developed by Montal and Mueller which rely on the formation of a lipid bilayer across a small aperture so that specific proteins of interest can be inserted [3]. In our initial work, we demonstrated that we could replicate Teflon® apertures often used for the Montal-Mueller techniques on a silicon substrate using traditional microfabrication procedures [4]. These fabricated apertures had a diameter of 150μm and functioned similarly to commercially available products.

Both the commercially available Teflon® apertures and the microfabricated silicon apertures had drawbacks which prevented their use as a long-term sensing substrate, including the mean time to failure of the membranes and the painting techniques needed to form the bilayer. We have developed a fabrication sequence used to manufacture sub-100nm pores in a silicon substrate in an effort to increase the longevity and robustness of reconstituted lipid bilayers. This reduction in pore diameter facilitates the use of vesicle fusion as a membrane formation technique and will also increase the membrane lifetime.

Commercially available silicon-on-insulator wafers with a diameter of 100mm, consisting of a sandwich of a 450μm thick “handle” wafer, a “buried” silicon dioxide (SiO₂) layer of 1μm and a silicon “device” layer of 340nm where used for fabrication of the nanopore. The wafers were initially oxidized to form a thin 65nm SiO₂ hard mask. 3% polymethyl methacrylate (PMMA) in anisole was spun on the top “device” layer of the wafer, in which 100nm circles were electron beam patterned in a JEOL JBX-6400. The SiO₂ hard mask was then etched in an Oxford 80+ reactive ion etch tool (RIE) using CHF₃:Ar , followed by the etching of the top “device” layer in a STS Inductively Coupled Plasma (ICP) RIE using Cl₂ gas chemistry. The backside of the wafer was then patterned with 100μm circles in a thick positive photoresist, AZ 4620 and then etched down to the “buried” SiO₂ layer in an STS ICP etcher using the Bosch process [5]. The wafer was then thoroughly cleaned, followed by a directionally selective wet etch of the “buried” SiO₂ layer in buffered oxide etchant, thus completing the fabrication of the pore. Finally, the device was thermally oxidized in a dry atmosphere to controllable reduce the size of the nanopore to a final radius of 20nm.

This high yield and robust process flow will enable the formation of silicon nanopore arrays for a variety of biological sensing and instrumentation applications. We will present our latest results including impedance spectroscopy analysis of the arrays coated with black lipid membranes.

Fig. 1 Shows a cross-sectional image of an array of cylindrical nanopores in the device layer of an SOI wafer. Pores in this image have a diameter of approximately 40nm.