Materials for advanced gate stacks in CMOS

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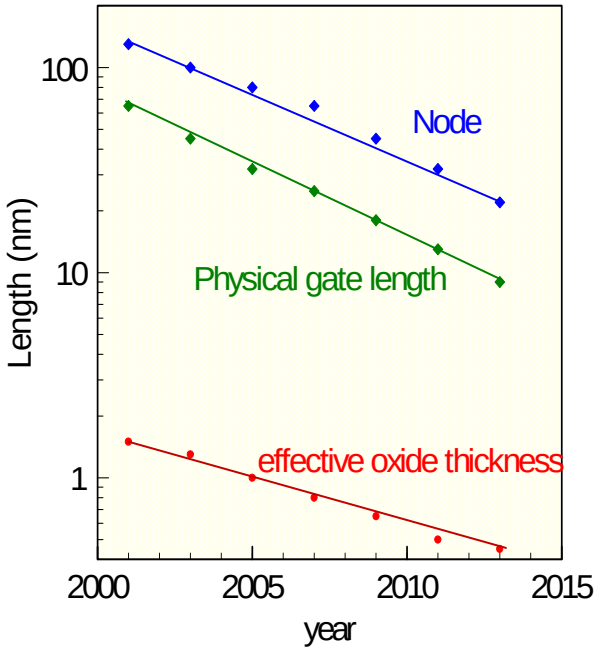
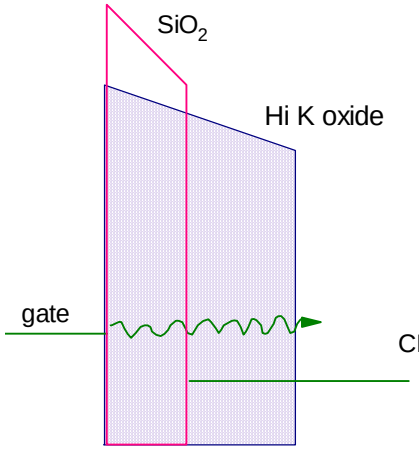
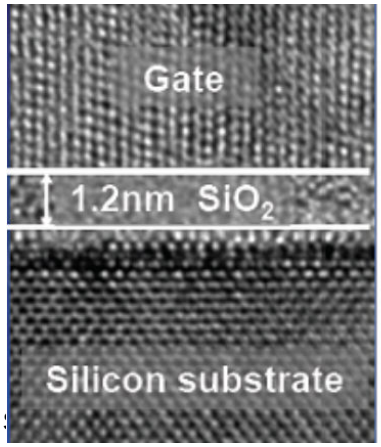
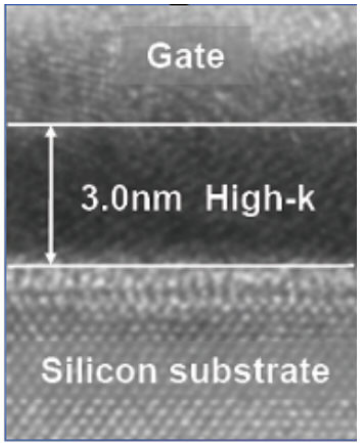
- why – High K oxides / Metal gates
- Choice of gate oxide – HfO_2
- Defects and trapping
- Mobility
- Metal gate choice
- ‘Fermi level pinning’

Scaling and high K oxides





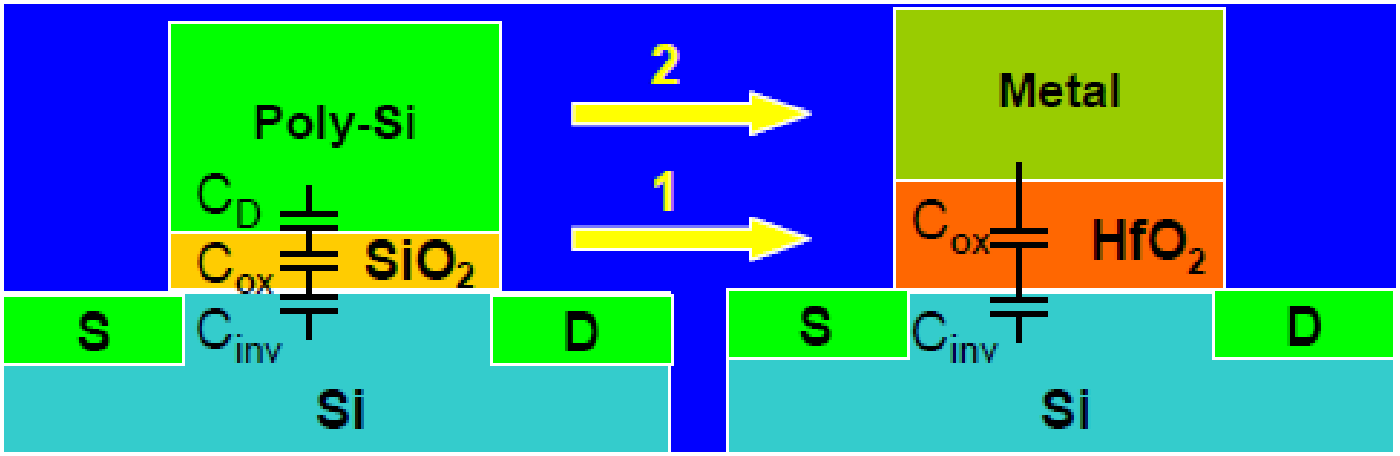




- SiO_2 layers <1.6 nm have high leakage current due to direct tunnelling.
- Replace SiO_2 with physically **thicker layer** of new oxide with **higher K**
- Maintain C/area

$$C = \frac{K\varepsilon_0}{t}$$

Metal Gates



- replace doped poly-Si gate with metal gate of higher electron density
- to remove its depletion width, reduce T_{inv}

CMOS Periodic Table, 1970's

1A	2A	3B	4B	5B	6B	7B	8B			1B	2B	3A	4A	5A	6A	7A	8A
H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg											Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ce															

- CMOS was once very conservative - no new materials

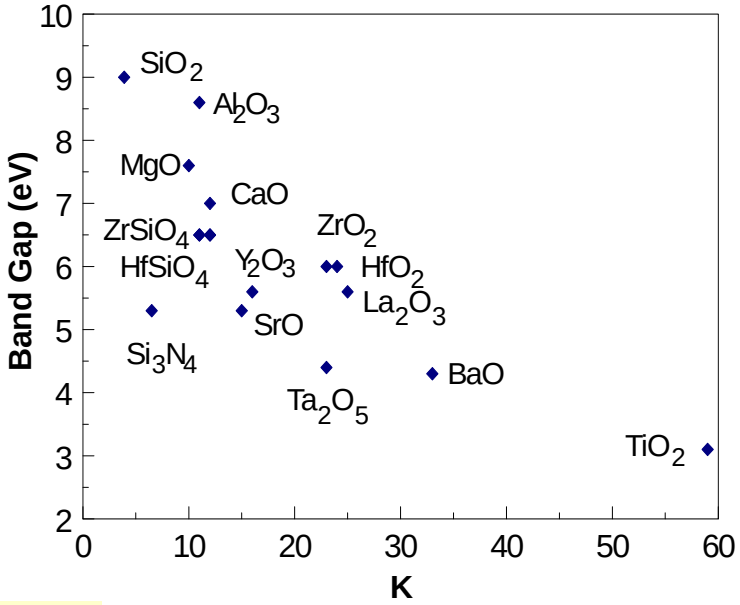
CMOS Periodic Table, 2000's

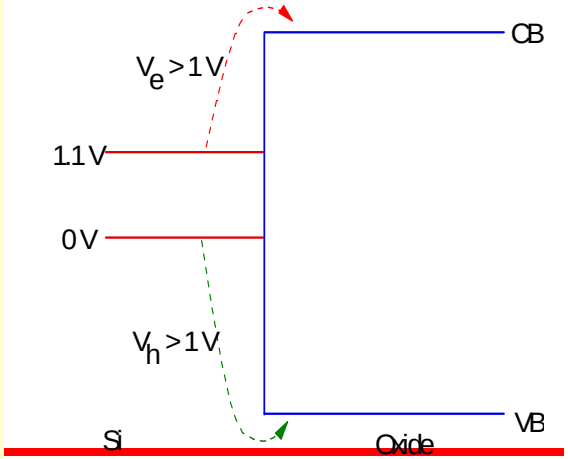
1A	2A	3B	4B	5B	6B	7B	8B			1B	2B	3A	4A	5A	6A	7A	8A
H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg											Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ce															

- Now most elements usable

Requirements for High K oxide (2000)

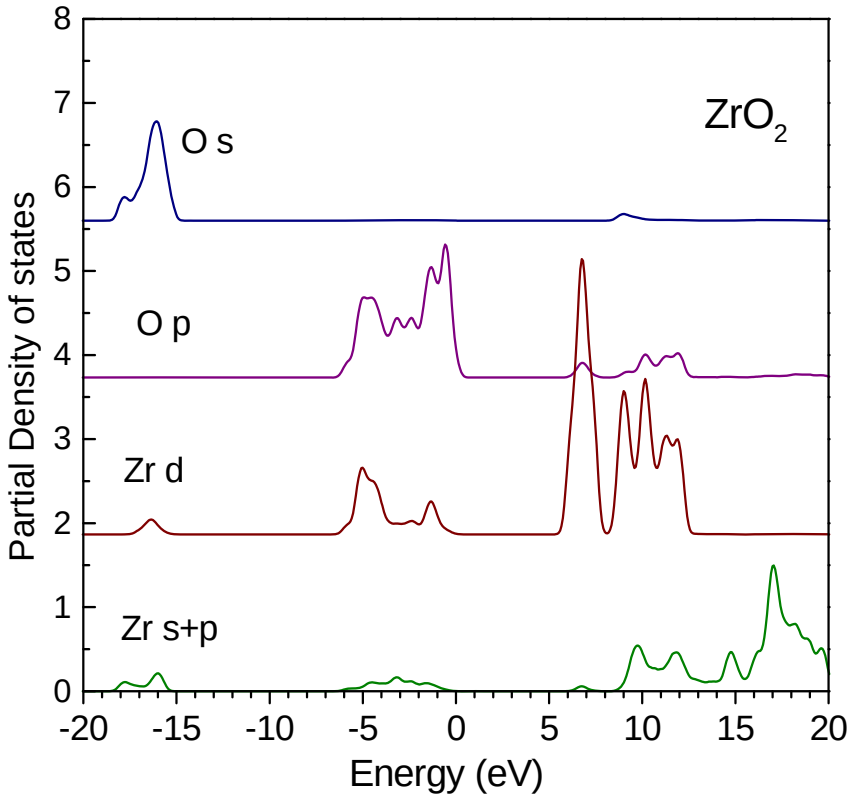
- **Thermodynamic stability**, no reaction with
  $MO_x + Si = M + SiO_2$
  $MO_x + Si = MSi_y + SiO_2$
  Hubbard and Schlom, J Mater Res 11 2757 (1996)
- **Withstand 5 second anneal at 1000C.**
  - No crystallisation, low O diffusion rates..
- **Good interface with Si**, few defects
  - Amorphous or epitaxial
- **Potential Barriers** – band offsets
  J
- Allows - Hf, Zr, Al, Sc, Y, La, lanthanides





CUED

What is a high K oxide ?

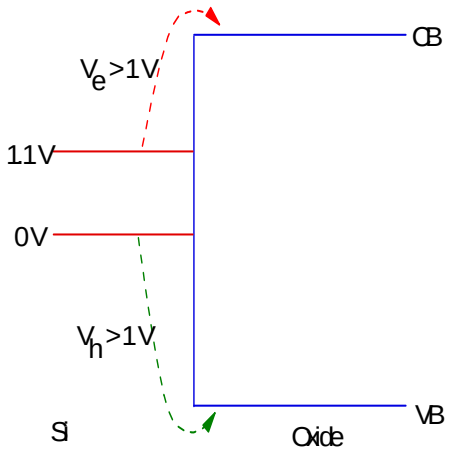


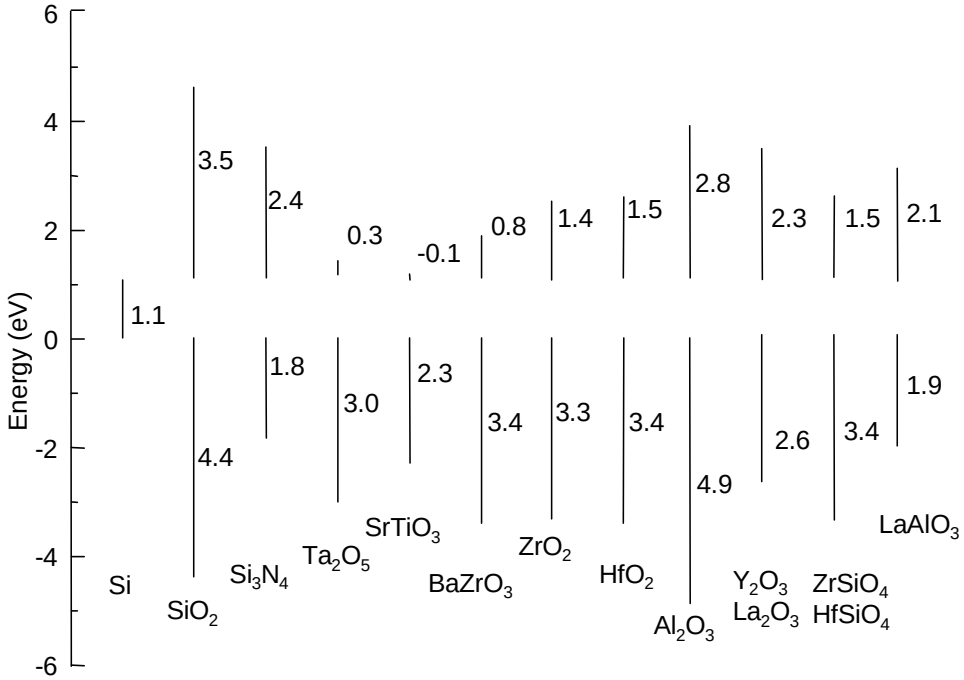
- closed shell transition metal oxide
- Valence band = O 2p
- Conduction band = Zr d
- Gap = 5.8 eV
- Large dielectric constant arises from lattice modes

$$\varepsilon_0 = \varepsilon_{electronic} + \varepsilon_{lattice}$$

$$\varepsilon_0 = n^2 + \frac{Ne^2 Z^{*2}}{m\omega_{TO}^{\ 2}}$$

Band offsets predicted by Schottky barrier theory



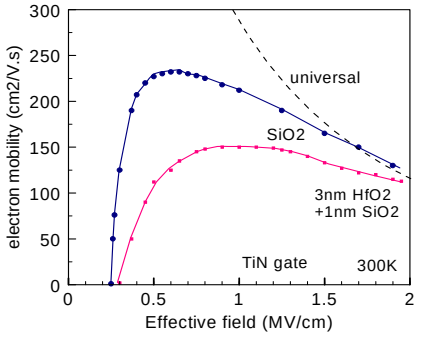


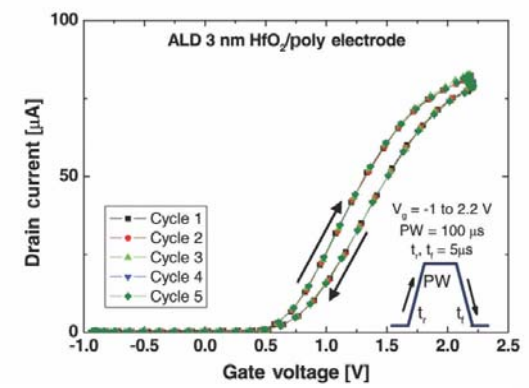
- band offsets calculated by MIGS model
- $\phi_{\beta n} = S(\phi_m - \phi_{CNL}) + (\phi_{CNL} - \chi)$
- S = 0.5 for HfO_2 in MIGS ($\varepsilon_\infty = 2$)
- Robertson, J Vac Sci Technol B **18** 1785 (2000)

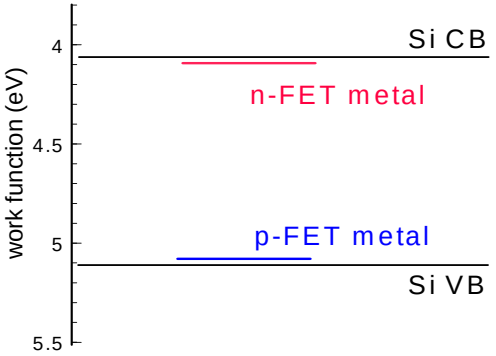
	Calculated	Experiment	Ref
Ta_2O_5	0.35	0.3	Miyazaki JVST2002
$SrTiO_3$	-0.1	<0.1	Chambers, APL 77 1662 (2000)
ZrO_2	1.4	1.4 2.0	Miyazaki Afanasev, JAP 2000
HfO_2	1.4	1.2	Garfunkel, APL 2002
Al_2O_3	2.8	2.8	Ludeke, APL 76 2886 (2000)
$LaAlO_3$	1.0, 2.1	1.8	Edge, APL (2004)
Y_2O_3	2.3	1.6	Miyazaki
La_2O_3	2.3	2.3	Hattori (2004)

4 problems with high K oxides

1. Scaling to smaller EOT, higher K
2. Low Carrier Mobility esp n-type
3. Charge trapping - V_T shifts
4. V_T control - Fermi level pinning for metal gates, esp PMOS

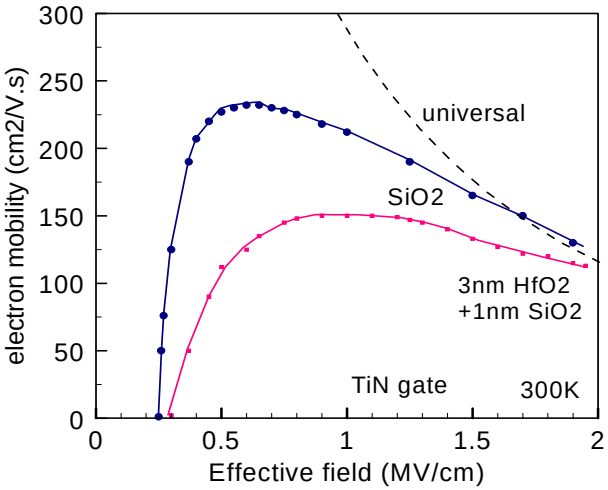


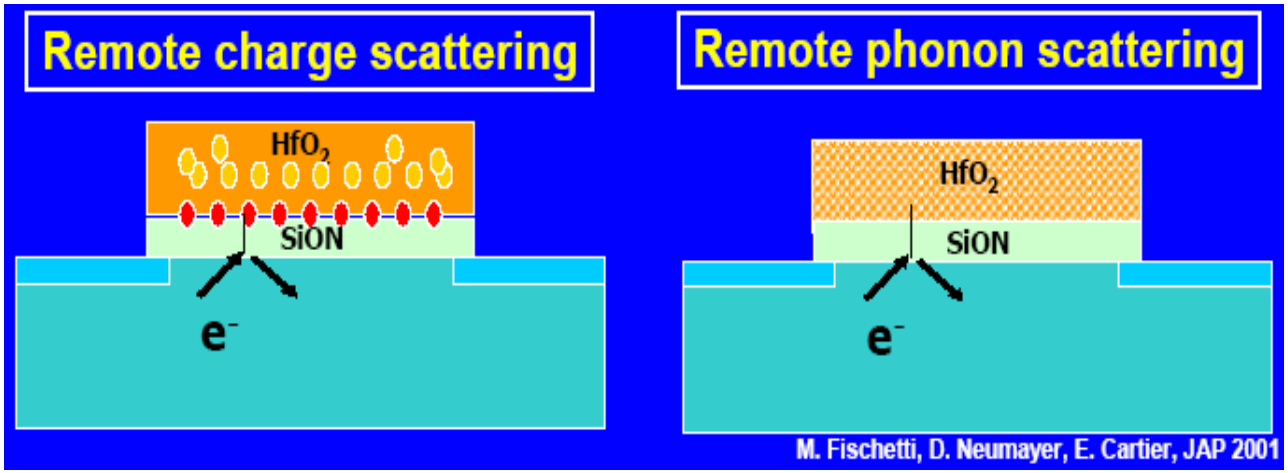




Channel mobility

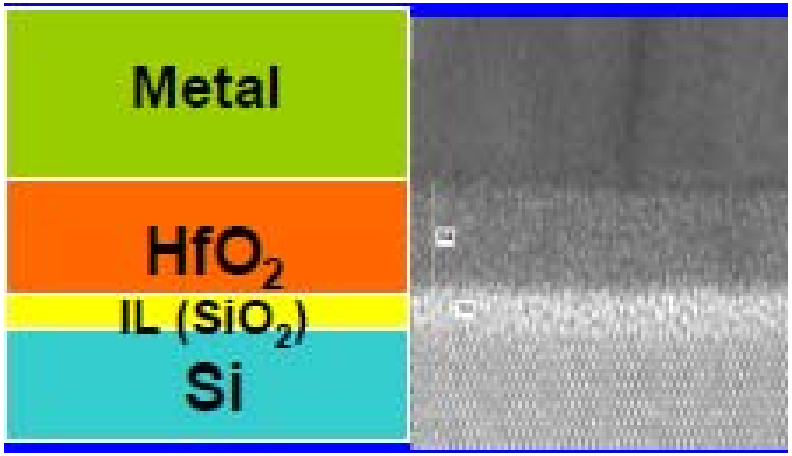
- Mobility of FETs with high K oxides was below ‘Universal mobility model’ value
- Due to scattering by defects and by optical phonons in oxide

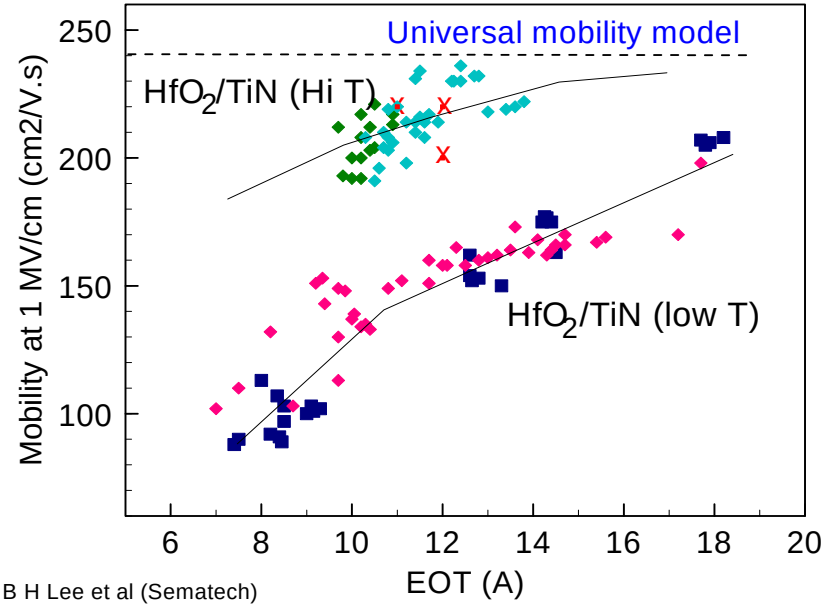




How to improve mobiliy

- Separate HfO_2 from channel by 1 nm of SiO_2 improves mobility by screening remote scattering
- K Maitra,..IBM, JAP (2007)

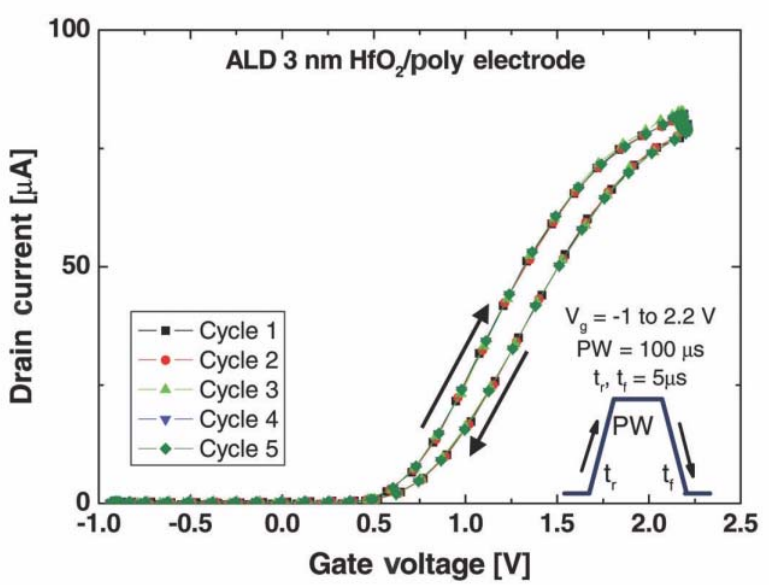


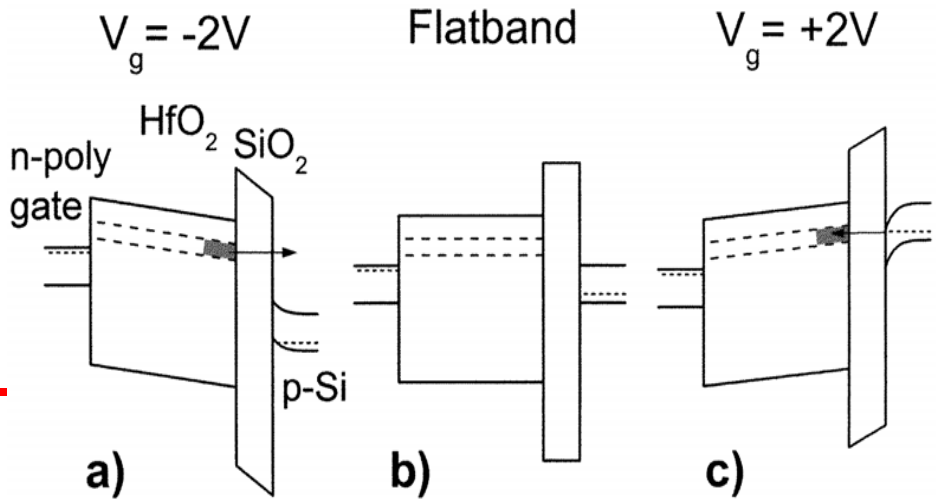


B H Lee et al (Sematech)

Defects and Trapping

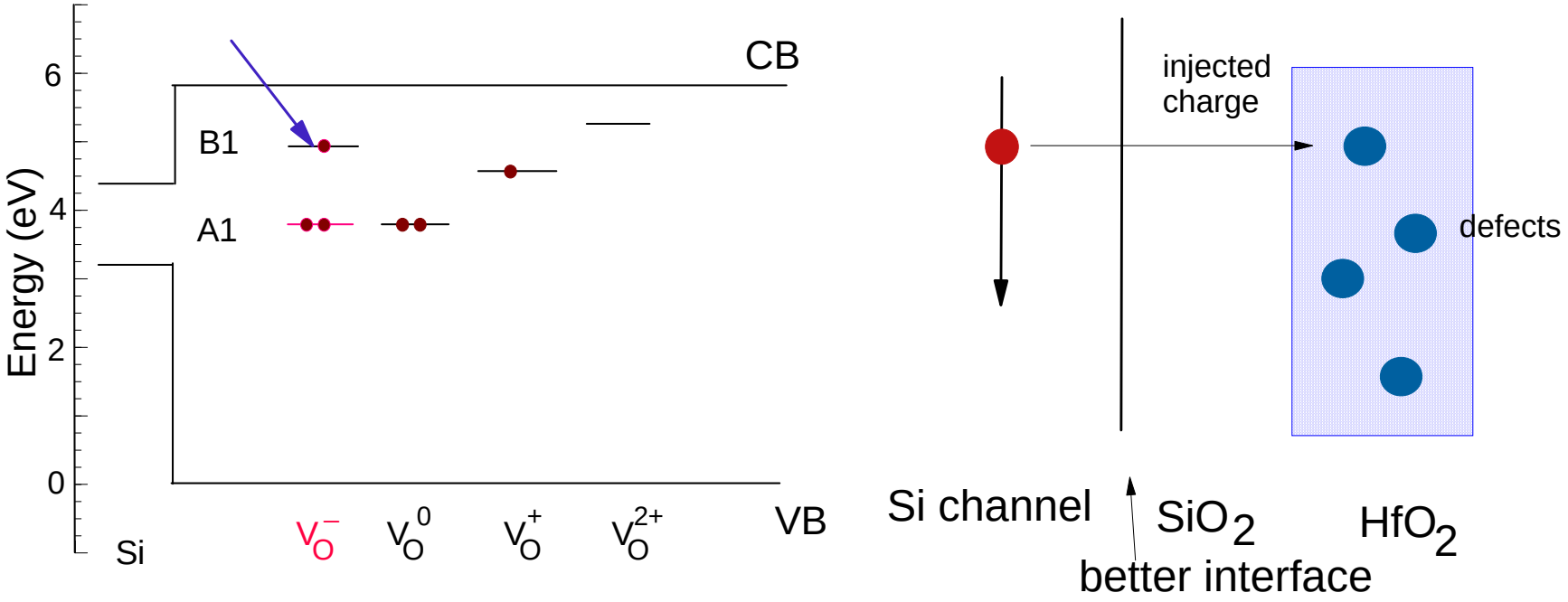
- Defects cause charge trapping and transient V_T shifts
- Due to defect band close to Si CB





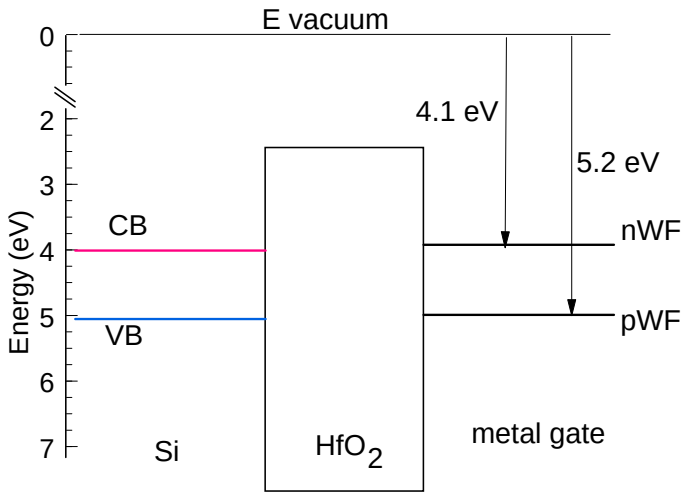
Oxygen vacancy problem

- Oxygen vacancy level gives negative state near CB (calculation, with correct band gap; Xiong, Robertson, Clark, APL 2005)
- Separate HfO_2 from channel by 1 nm of SiO_2
- Passivate by fluorine



Gate work functions for n- and p-FET

$$V_{FB} = \phi_{gate} - \phi_{Si} - Q_f / C_{ox}$$



- Small gate threshold voltage (V_T) requires gate work functions similar to Si band energies

Periodic Table

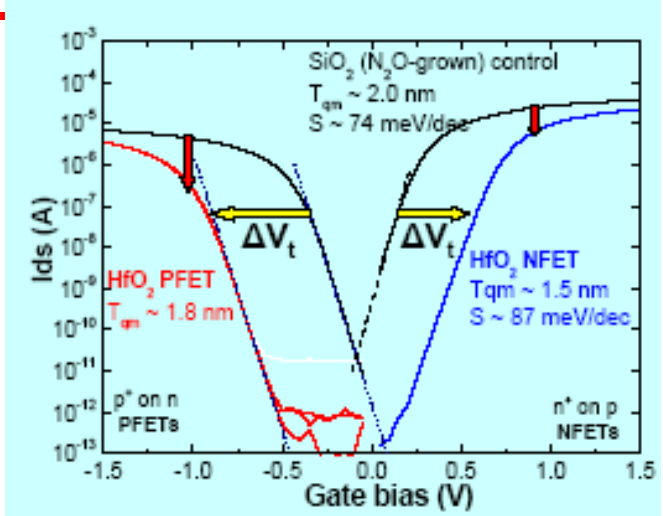
1A	2A	3B	4B	5B	6B	7B	8B			1B	2B	3A	4A	5A	6A	7A	8A
H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg											Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ce															

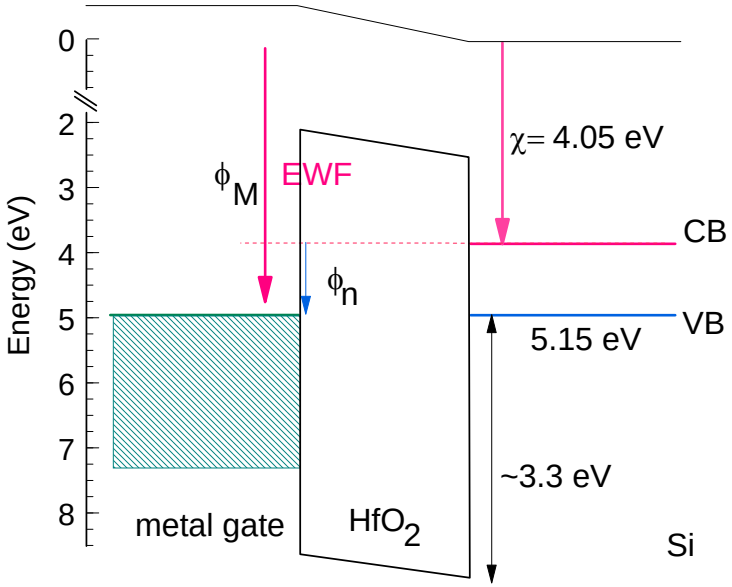
lanthanides

- Few metals have Φ <4.0 eV or > 5.1 eV
- and compatible

Gate Work functions

- In addition, High K oxides suffer from ‘Fermi level pinning’
- Schottky barrier height ϕ_n of metal depends on charge transfer at interface
- $\phi_n = S(\phi_M - \phi_{CNL}) + (\phi_{CNL} - \chi)$
- Pinning factor S
  - $S = d\phi_{bn}/d\phi_M$
- Interface gap states can pin E_F

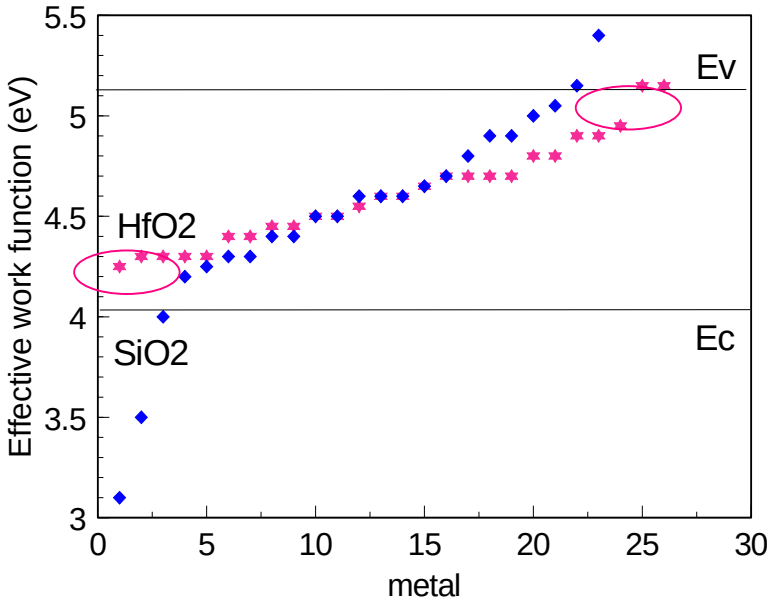


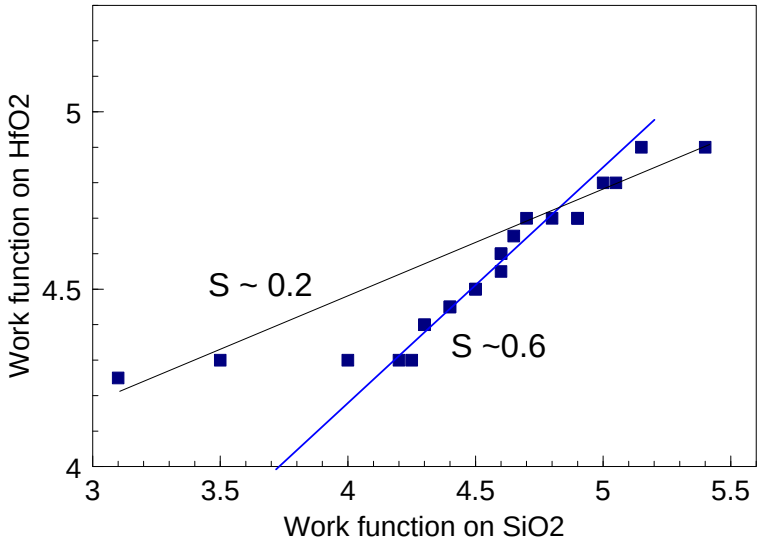


CUED

WF data for gate metals on annealed HfO_2

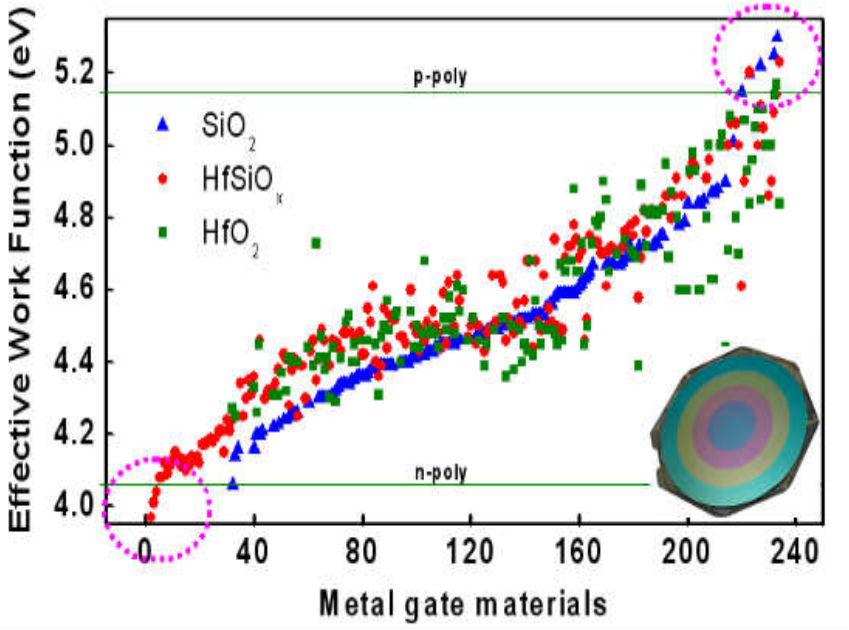
- Metal – oxide – channel subjected to 1000C activation anneal, causes strong WF changes
- Difficulty of finding metals with n- and p-type EWF on HfO_2
  - Schaeffer, IEDM (2004)
- S = 0.5 for HfO_2 in MIGS (ε_∞ = 2)
- EWF on HfO_2 and SiO_2 vs metal
  - Redraw as EWF vs WF assuming S = 1 for SiO_2

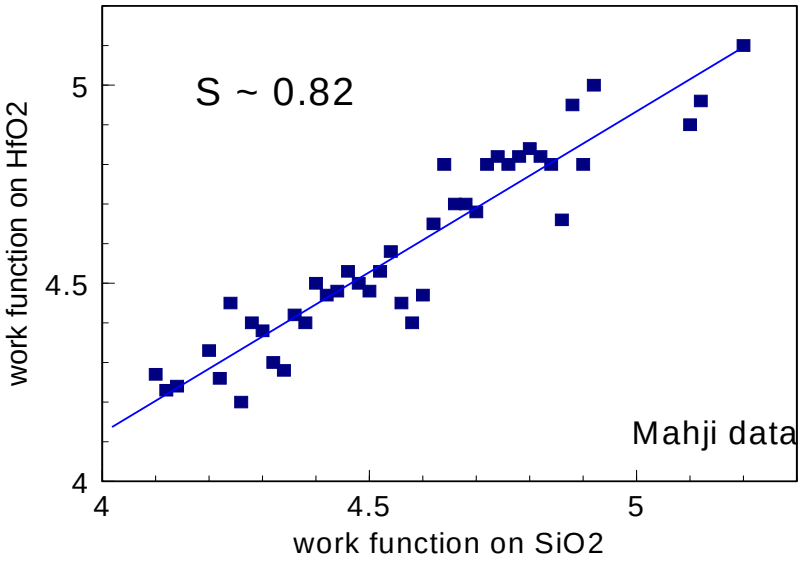




EWF of gate metals

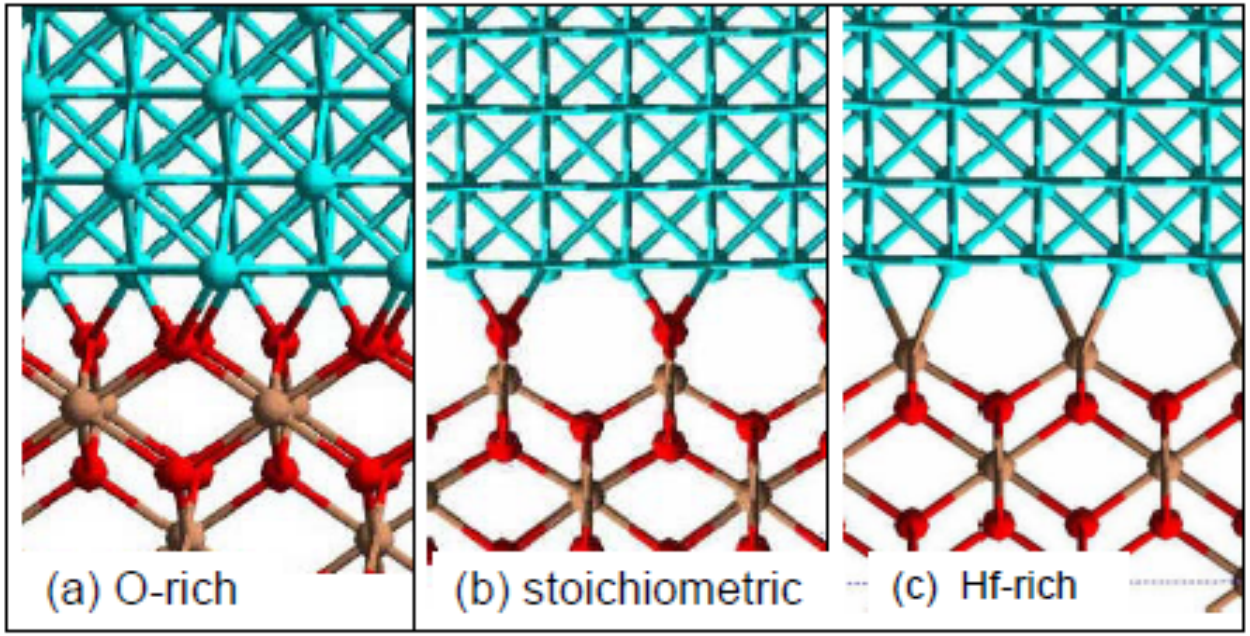
- EWFs now reach Si VB, CB
- More refractory metals
- Terraced oxide allows better WF extraction
- H C Wen, Microelec Eng (2007)
- Similar EWF for SiO_2 and HfO_2
- Redrawn assuming S=1 for SiO_2 gives S ~0.82





Intrinsic
Full calculation of metal - HfO_2 interfaces

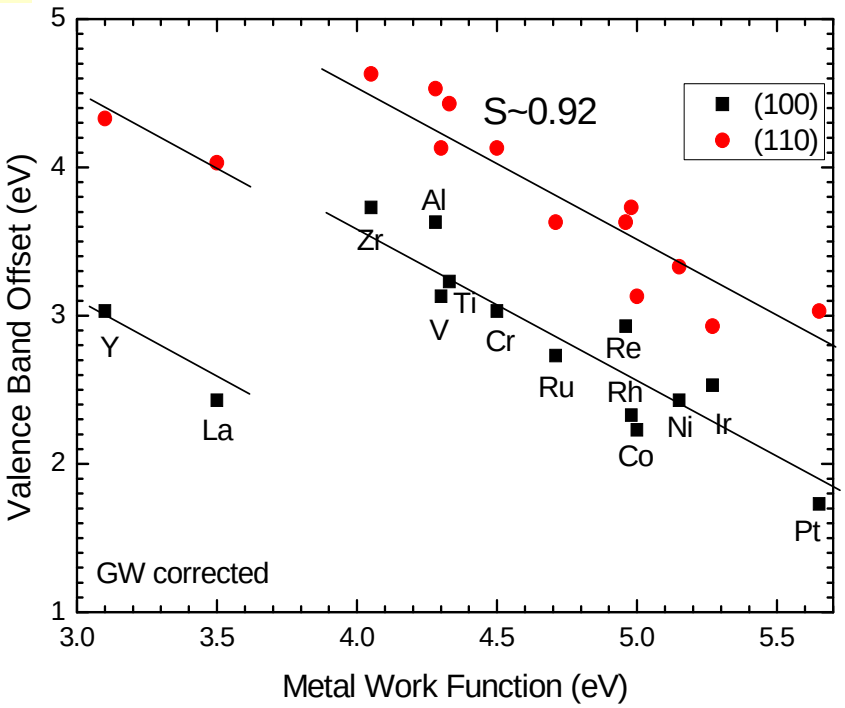
(100)HfO_2

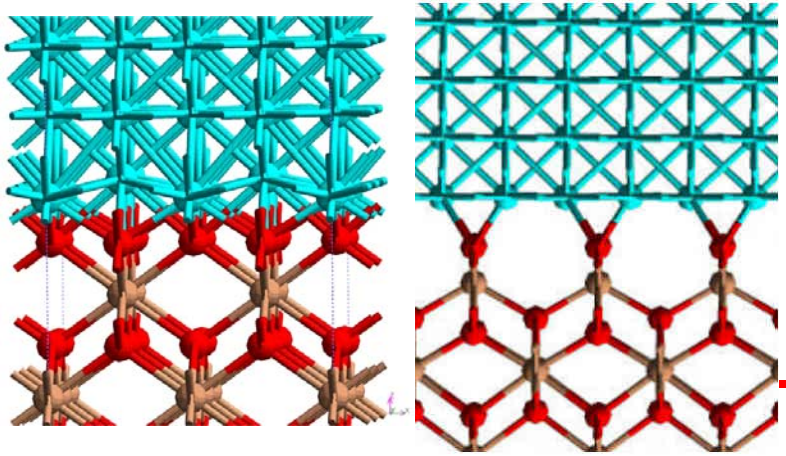


- Calculate Barrier heights (VBO) for supercell models of various metals on cubic HfO_2
- [100]Ni // [110]HfO_2 45^0 rotation
- K Tse, J Robertson, Phys Rev Lett **99** 086805 (2007)

Barrier heights - unpinned

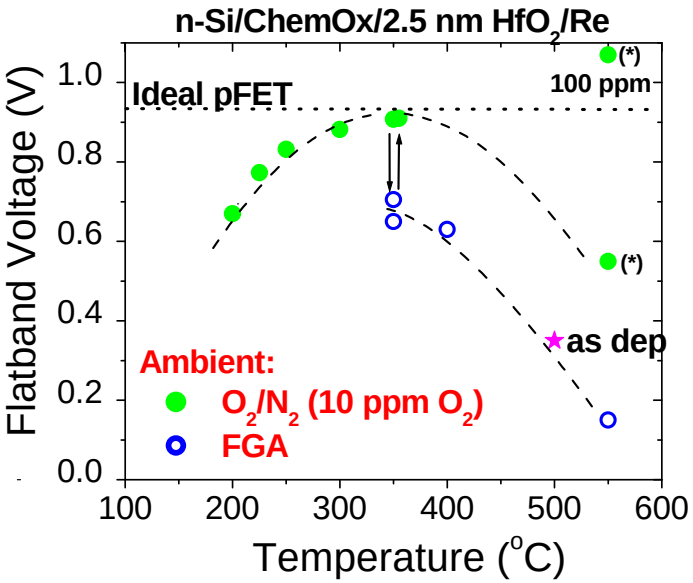
- Slope S = 0.92 UNPINNED
- **No intrinsic pinning**,
- VBO for O-rich (100) less than (110), due to extra dipole
- O -rich has larger EWF
- VBO depends on interface polarity





Extrinsic
High WF metals on HfO_2

- High work function pFET metals during annealing
- Pinning on high WF metals occurs only after >400C annealing
  - Cartier, SSDM 2005, Schaeffer, APL 2004)
- *Reversible shifts* - extrinsic
- Re, Pt, Ru, W all have O permeability
- Mechanism ?

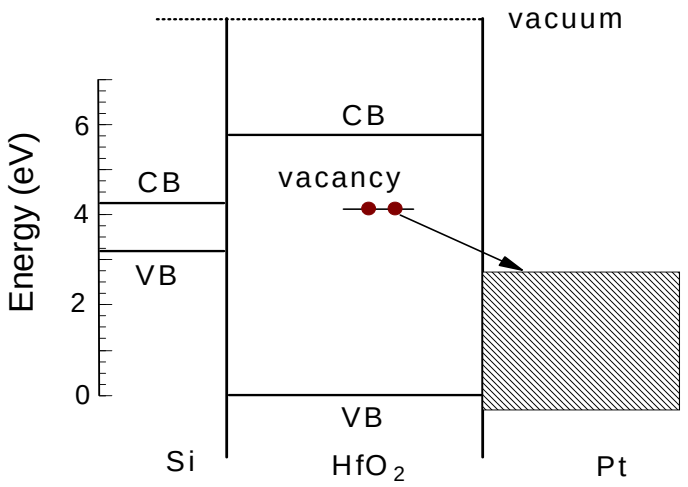


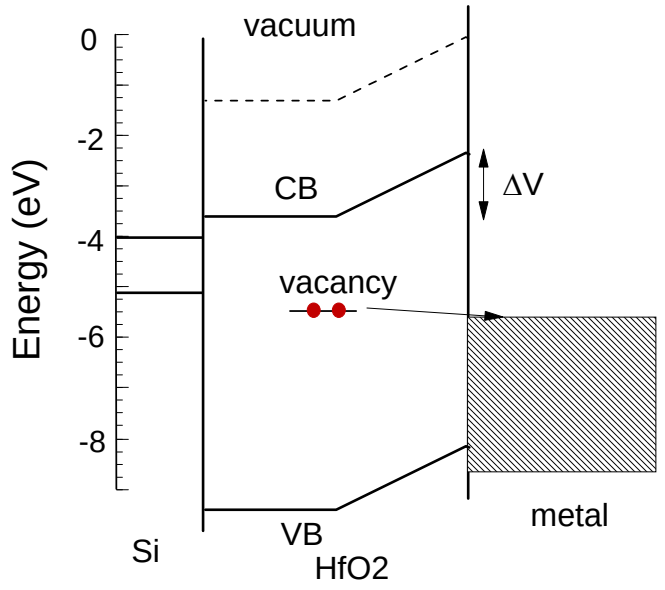
Mechanism - oxygen vacancy

- Oxygen vacancies V_O^0 has gap state above metal E_F
- Electrons fall to metal E_F - band bending
- V_O could cause pinning by band-bending in oxide

- But O vacancy costs 6.4 eV wrt O_2 (Scopel et al, APL 2004) – too costly
- *Should not be not relevant*

- $n = n_0.\exp(-\Delta G/kT)$
- Need $\Delta G < 1$ eV for $n \sim 10^{20}$ cm^{-3} with kT~0.1 eV, T=1000C

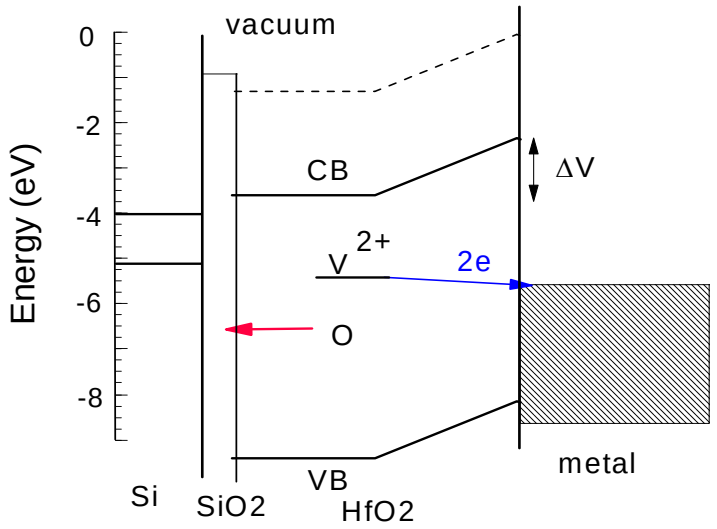


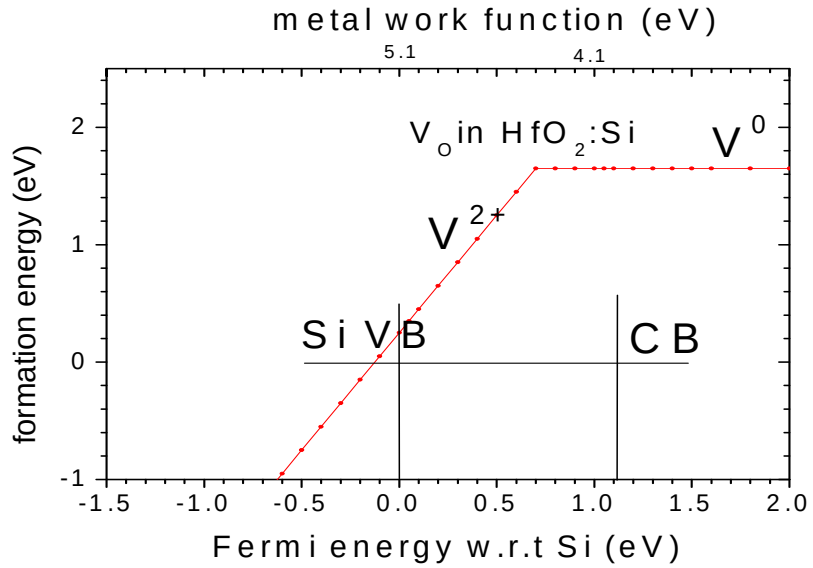


CUED

O vacancy with SiO_2 formation

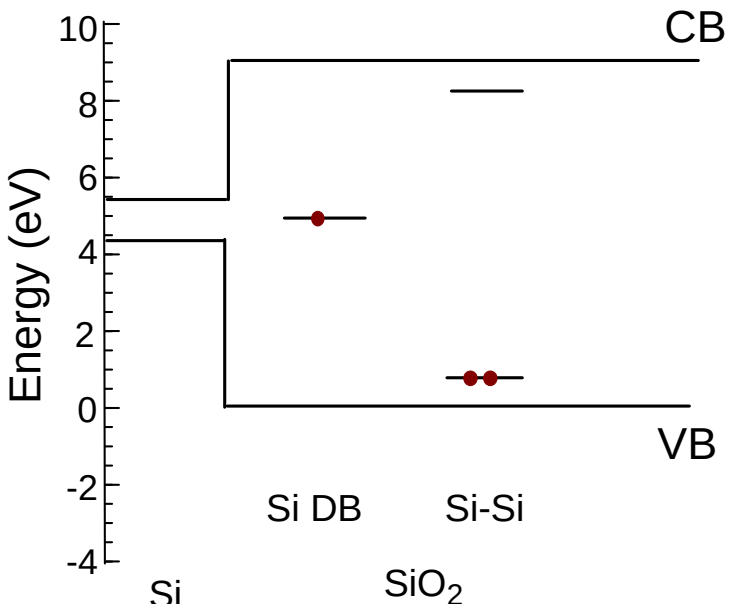
- React O with Si
- $O_O + ½\ Si = V_O^{2+} + ½\ SiO_2 + 2e^-$
- $\Delta G_3 = \Delta G_1 + G(½SiO_2)$
- $= 6.4 – 4.73\ eV – q(E_{vac}–E_F)$
- gains 4.73 eV by forming SiO_2
- ΔG = negative at E_F = -0.15 eV, many vacancies can form
- Bend-bending causes E_F pinning
  - Akasaka, JJAP 45 L1289 (2006)
  - Robertson, Sharia, Demkov, APL 91 132912 (2007)

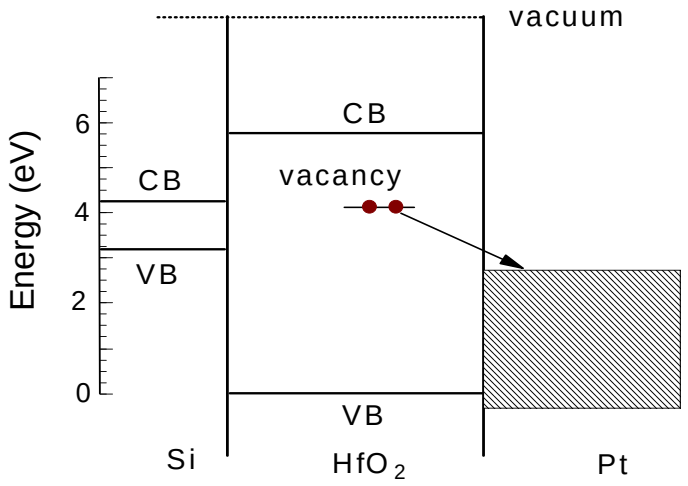




SiO_2

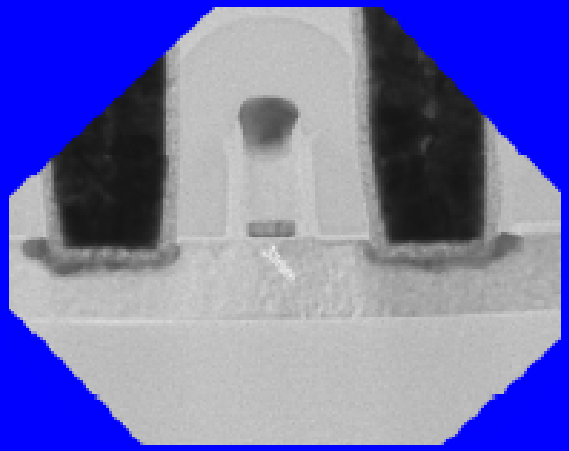
- Why didn't this problem occur with metals on SiO_2?
- V_O in SiO_2 is Si-Si bond, with states near VB and CB, whereas HfO_2 has filled state just above midgap





Gate flows

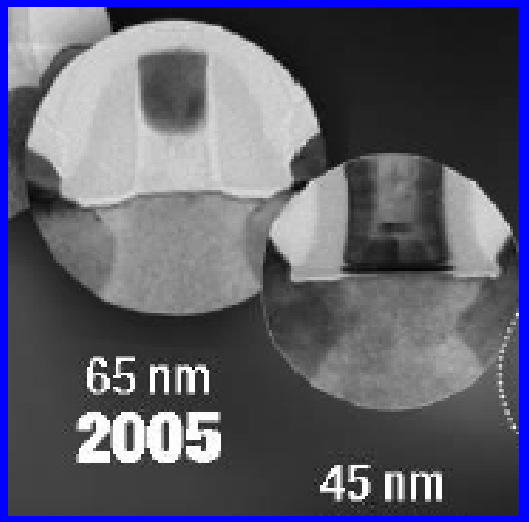
Gate first
(IBM alliances)



Conventional high-T process

Process flow differs only in the gate stack module

Replacement Gate
(INTEL Corp., website)

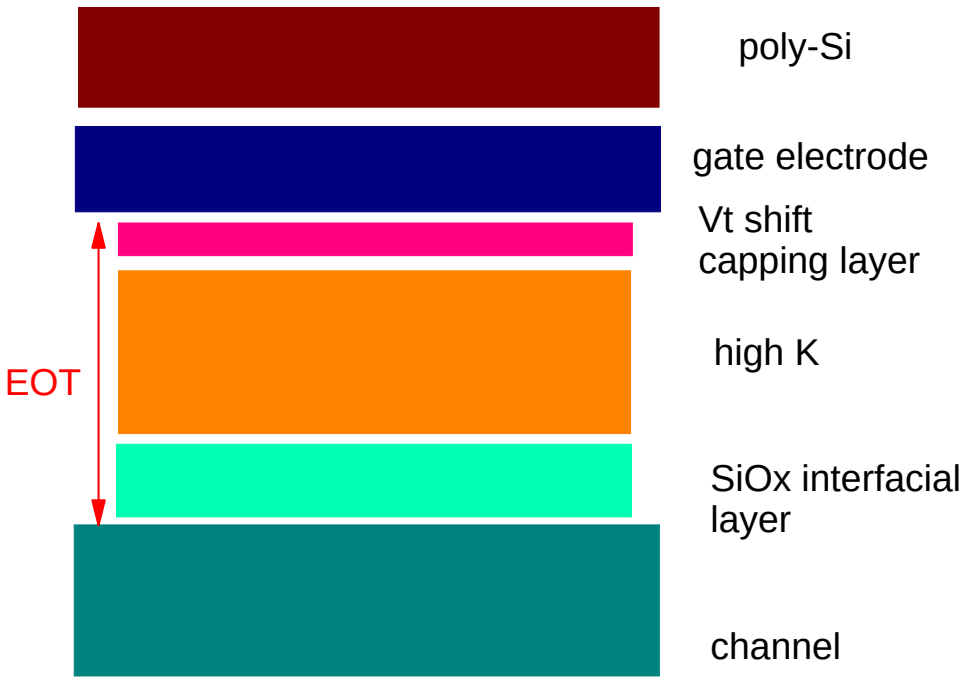


Conventional high-T process
+ Low-T replacement gate process

Process flow differs substantially from traditional approach

General conclusions - Nano-laminates

- CMOS gate stacks are nano-laminates
- Not semi-infinite layers and substrates
- Each layer has a function
- Reactions occur over 1 nm



Conclusions

- High K /metal gate requires many elements
- Mobility degradation, trapping problems solved
- High WF metals pinned on HfO_2:M interfaces by reversible O vacancies and band-bending