

# Practical redundant designs for nano-architectures: Review of novel theoretical and simulation results

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In this tutorial article, we explore the feasibility of designing reliable nano-architectures using practical/economical (i.e., small = “less than 100”, and very small = “less than 10”) redundancy factors. To this end, we begin with a thorough review of redundant design strategies for fault-tolerant nano-architectures. We then adapt three redundant design strategies - modular redundancy, von Neumann multiplexing, and reconfigurability - to majority-gate circuits, and analytically evaluate these designs’ reliabilities for small redundancy factors (including fractional factors between one and two), using exact combinatorial arguments as needed. Our analysis of von Neumann multiplexing motivates several extensions that allow optimization of reliability for very small redundancy factors, and highlights the benefit of using majority-gates in nano-scale design, paving the way for practical fault-tolerant architectures. Next, we postulate redundant architectures that mesh multiple design strategies. Using these meshed strategies, we study the feasibility of achieving chip-level reliability with very small redundancy factors, given estimates on device failure probabilities. Finally, our redundant designs are compared with previous studies of redundant architectures using the Nanoprism model-checking tool. In exploring the feasibility of redundant designs, we also thoroughly review the analytical methods that have been used to characterize reliability of fault-tolerant architectures in general. This tutorial is organized as follows: In Section I, we review relevant literature on the design of reliable (fault-tolerant) logic circuitry. We primarily focus on the literature concerning development and analysis of practical redundant design schemes for fault-tolerant nano-architectures, but also discuss theoretical studies on optimal redundant design of reliable logic functions. In reviewing the existing literature, we identify needed directions for further study, stressing in particular the importance of considering non-Boolean gates in general, and majority-gates in particular, and for studying practical/economical designs i.e., those that require only small or very small redundancy factors. In Section II, we describe adaptation of redundant design strategies, and their analytical analysis, to majority-gate circuits. In Section III, we present some novel redundant design strategies that are motivated by our study of enhancing von Neumann multiplexing, at small and very small redundancy factors, and we detail simulation results for 100 nm CMOS, as well as for single electron technology. In Section IV, we assimilate multiple strategies for redundant design (including device level ones), to explore feasibility of combining them for lowering the redundancy factors even more. We also discuss simulation tools for efficient calculation of reliabilities for such designs.

The tutorial covers 50 years, and will include about 150 references.

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