

Transistor elements for 30 nm physical gate lengths and beyond

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Transistor scaling issues have been examined to determine the implications on device performance. We have fabricated planar Si transistors down to 10 nm physical gate length using a special spacer gate technique. Transistors at these aggressively scaled dimensions down to 15 nm are shown to exhibit good device characteristics. Although transistors with 10 nm physical gate length show normal switching characteristics, they exhibit very high off-state leakage. To alleviate the high parasitic leakage problem, we have demonstrated a transistor structure with a fully depleted substrate (DST) providing near-ideal sub-threshold gradient and highly reduced DIBL (drain induced barrier lowering). In addition to DST device architecture, new electronic materials and modules will be needed in the future to maintain high performance and low parasitic leakages.

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