Strategies for nanoelectronics

G. F. Cerofolini [a,*], D. Mascolo [b], V. Nosik [c]

[a] *STMicroelectronics, Stradale Primosole 50, 95100 Catania CT, Italy.*

[b] *STMicroelectronics, Via Remo De Feo 1, 80022 Arzano NA, Italy.*

[c] *STMicroelectronics, Posledny Pereoulok 11/1, Moscow 103045, Russia.*

Denoting with 'nanodevice' any device with size in an one dimension at least in the nanometre length scale (NLS), the basic constituent of integrated circuits (ICs), the metal-oxide-semiconductor (MOS) field-effect transistor (FET), is by several years a nanodevice. In fact, the thickness of the SiO_2 gate dielectric is around 3 nm for logics or 5 nm for memories. However, since the factors limiting the IC integration are horizontal sizes, in electronics one speaks of nanodevice when its size in one horizontal dimension at least is in the NLS.

The definition of features in the NLS is impossible via optical lithography, but can be done using electron- or ion-beam lithography. These techniques, however, are very expensive and still in their fancy, at least for what concerns their exploitation in the industry practice.

Geometries in the NLS can however be produced with relative ease by transforming vertical features (like film thickness) in the vicinity of a step of a sacrificial layer into horizontal features. The ultimate length producible in this way is controlled by the steepness of the step defining the sacrificial layer and the uniformity of the deposited or grown films.

While useful for the preparation of a few devices with special needs, the above trick does not allow by itself the development of a nanotechnology, where *each layer* useful for defining the FET should be in the NLS and aligned on the underlying geometries with tolerances in the NLS.

Setting up such a nanotechnology is a major technological problem which will involve the IC industry in the post-RoadMap era. Which materials, geometries and alignments are required for the preparation of nanoICs is manifestly largely unpredictable. Nonetheless, the assignment of technological goals (able to clarify which difficulties will be met in the long road to nanoelectronics and which technologies should be developed for that) is certainly useful. Irrespective of the detailed structure of the basic constituents of nanoICs (molecules, supramolecular structures, clusters, etc.) any nanoIC can hardly be prepared without the ability to produce arrays of conductive strips with pitch in the NLS. This work is devoted to describe a scheme (essentially based on the existing microelectronic technology) for their production without the use of electron- or ion-beam lithography and how it can be used to host molecular devices.

---

* Corresponding author. Tel. +39-039-6037023. FAX +39-039-6037030.
Email address: gianfranco.cerofolini@st.com (G. F. Cerofolini).