NanoCMOS simulation: Every atom counts.

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In the past couple of years CMOS (complimentary metal-oxide semiconductor) technology has become a true high volume nanotechnology with $40 - 50$ nm physical gate length devices available now in the 90 nm technology node [1] and 4 nm, MOSFETs demonstrated in a research environment. The 2003 edition of the International Technology Roadmap for Semiconductors forecasts that the mass-produced metal-oxide semiconductor field effect transistors (MOSFETs) will reach 7 nm gate length by 2018.

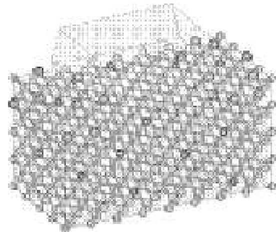

Fig. 1. Atomic structure of a 4 nm MOSFET with random dopants in the channel and in the source/drain region. For comparison a carbon nanotube and a channel protein are shown to scale on the same picture.

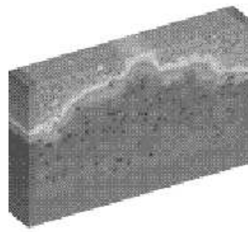

Fig.2. Potential distribution in a 35 nm MOSFET in which the detailed positions of dopants are considered.

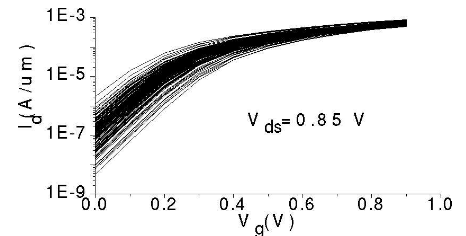

Fig. 3. Characteristics from 200 macroscopically identical 35 nm MOSFETs, obtained by 3D statistical 'atomistic' device simulation.

Nano-MOSFETs illustrated in Fig. 1, which are, for example, comparable in size to carbon nanotubes or channel proteins, will be extremely sensitive to individual discrete charges of dopants or trapped carriers. Trapping of a single carrier charge in defect states near the Si/gate dielectric interface and the related local modulation in carrier density and/or mobility will have a profound effect on the drain and gate current introducing low frequency (LF) noise with large magnitude [2]. Intrinsic parameter fluctuations associated with random discrete dopants, interface roughness and line edge roughness (LER), present increasing problems to the integration of nano-MOSFETs in a billion transistors count chips [3].

In this paper we present coherent approaches to the simulation of atomic scale effects and intrinsic parameter fluctuations in nano-CMOS devices based on classical, Monte Carlo and quantum mechanical techniques. We also illustrate how the intrinsic parameter fluctuations in such devices affect the yield and the functionality of the corresponding circuits and systems using stochastic Spice simulations.

[1] T. Schafbauer, et al, Symposium on VLSI Technology, Digest of Technical Papers, p.62, 2002

[2] A. Asenov, R. Balasubramaniam, A. R. Brown and J. H. Davies, IEEE Trans. Electron Dev., Vol.50 p.839, 2003

[3] A. Asenov, et al, IEEE Trans. Electron Dev., Vol.50, pp.1837-1852, 2003

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