Electrical characteristics of core-shell p-n GaAs nanowire structures with Te as the n-dopant

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Photovoltaic (PV) devices employing semiconductor nanowires (NW) have the potential for lower cost and greater energy conversion efficiency compared to conventional thin film devices due to less material utilization, enhanced photovoltage or photocurrent due to hot carrier or multiexciton phenomena, enhanced light absorption, and freedom from lattice matching requirements due to strain accommodation at the nanowire surfaces. However, the current status of NW PV devices is far from satisfactory due to laboratory efficiencies that are still rather low. Hence, efforts are being made to improve their electrical characterization to give a more complete description of the device performance, which should be an important feedback to the fabrication procedure.

With this in mind, we have studied core shell GaAs NW structures for PV applications using impedance spectroscopy in the 10^3-10^7 Hz frequency range, for various applied DC biases. The structures consist of GaAs NWs grown by molecular beam epitaxy combined with a vapor-liquid-solid technique [1]. The NWs include a Te-doped (nominally n-type) core and a Be-doped p-type shell. Two samples (named A and D) were studied with two different Te-doped GaAs growth durations (5 and 15 min, respectively), in which the total (Te doped plus Be doped GaAs) growth duration was kept constant at 25 min. The use of Te instead of Si as the n-dopant comes from the amphoteric behavior that Si may have in GaAs NWs [2]. Further growth details and the DC I-V curves (which show reasonable p-n rectifying characteristics) of the samples studied here have been described elsewhere [1].

Figures 1(a), (b) show the impedance plots obtained with zero DC bias, for samples A and D, respectively. Both data sets show typical Cole-Cole behavior, as verified by fitting the corresponding theoretical expression [3] to them. However, the impedance values are much larger (about an order of magnitude) for sample D. This can be interpreted as due to a correspondingly much lower capacitance and larger AC resistance in this sample. The Cole-Cole behavior means that both samples behave as a set of relaxing dipole oscillators with a distribution of relaxation times (τ) about a mean value. We assume that these responses are dominated by charges at the p-n junctions. From the fit parameters, we deduce a wider τ distribution for sample D due to the larger interface disorder in this sample. The corresponding large AC resistance is then interpreted to be due to charge carrier localization (trapping) or scattering at disordered sites. The very low capacitance, in turn, could be due to either compensation and segregation effects at GaAs(Be)/GaAs(Te) interfaces induced by Te, which are most noticeable in sample D [1], or could reflect a smaller capacitance associated to the valley regions between NWs in this sample.

These results are currently being analyzed in terms of equivalent circuit models in an effort to isolate contributions to the impedance from different regions in the samples (the core-shell NW p-n interface, and the thin planar-like GaAs p-n junctions that develop at the valley regions between NWs, as observed in electron microscopy measurements). The outcomes of this analysis, which takes into account the effects of applied DC bias, and their impacts on device characteristics, will be discussed.

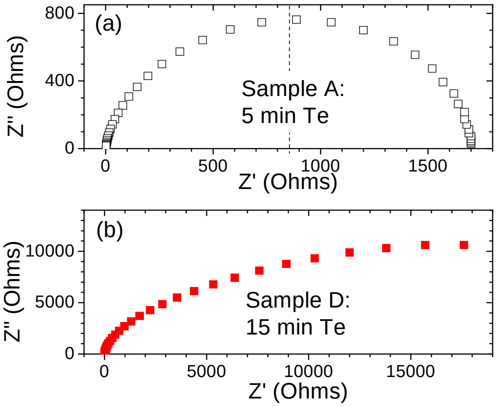

Fig. 1 Imaginary versus real impedance components for samples A (a) and D (b), respectively.

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