

# Capacitance optimization in commercial DRAM and Flash memory devices

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An ideal memory device would combine fast access with nonvolatility (long retention time). Currently, no design fulfills both requirements, and as a consequence the microelectronic industry has come to rely on two principal components for high-density storage: fast volatile DRAM and nonvolatile Flash products. Detailed structural analysis performed at Semiconductor insights (SI) on recently released sub-60nm DRAM and sub-50nm NAND Flash memories reveal interesting trends in the scaling-down of those devices. In this presentation, we focus on the manufacturers strategies to increase capacitance.

DRAM cells remain the high-density memory of choice for personal computers. A capacitor structure is the key component holding the charge in the memory cell. Initially, the capacitors were based on simple planar geometries with dielectric layers consisting of thermal silicon dioxide, but it has since evolved into three-dimensional structures with metal electrodes and high- $\kappa$  dielectrics, such as  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$ , and more recently  $\text{ZrO}_2$  [1]. In some devices, the capacitor architecture is based on the trench design, where deep and narrow holes are dug into the substrate. More commonly, it is based on the stacked design, where narrow tubular structures are formed on top of access transistors. Fig. 1 shows TEM images of stacked capacitors, where the high- $\kappa$  dielectric material between the TiN top and bottom plates appears clearly in (b).

Developments in Flash technologies continue to be driven by the increasing need for nonvolatile memory in portable devices such as mobile phones, mp3 players and digital cameras [2]. In a typical Flash cell, electrons are injected from the substrate into a floating gate (FG). The programming and erasing operations require the FG potential to be efficiently modulated by a control gate (CG). To increase the coupling ratio, the CG generally wraps around the FG and thin oxide/nitride/oxide (ONO) stacks are used

(Fig. 2). Recently, new high- $\kappa$  materials have been introduced for the intergate dielectric and the structure has been optimized.

In summary, for both DRAM and Flash memory devices, the continuing miniaturization relies on the introduction of new high- $\kappa$  materials and on the design of three-dimensional architectures. In the longer term, new concepts will need to be invented, in particular for sub-20nm devices, and technological innovations will therefore be critical to the future of memory technology [3].

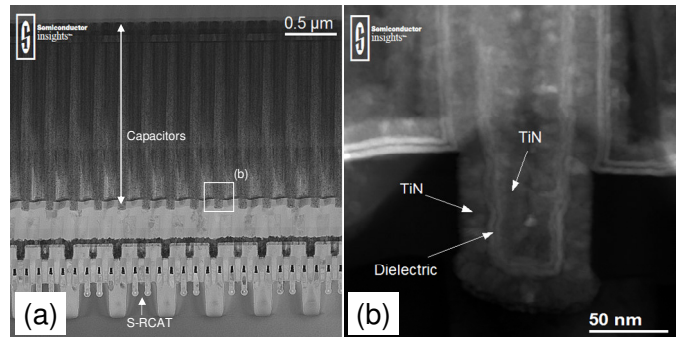


Fig. 1 Images of a DRAM with stacked capacitors taken along the bitline direction. (a) a low-resolution TEM image of the storage capacitor above the spherical-shaped recessed channel access transistor (S-RCAT). (b) an annular dark-field STEM image taken near the bitline contact where the high- $\kappa$  dielectric appears as a bright line between the top and bottom TiN electrodes. The approximate location of the image (b) is indicated in (a) by a square.

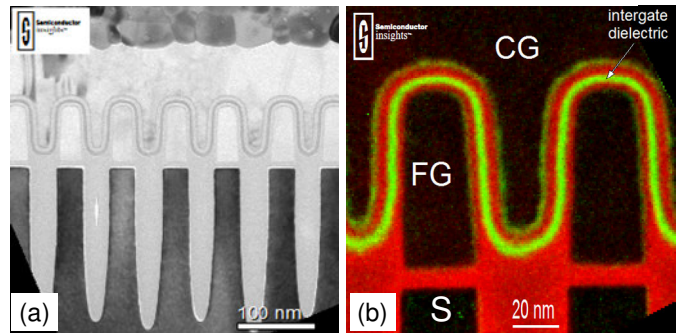


Fig. 2 Images of a floating gate NAND Flash device taken along the wordline direction. (a) a low-resolution TEM image and (b) a high-resolution energy-filtered TEM image. In the chemical map (b), the intergate dielectric, the floating gate (FG), the control gate (CG) and the substrate (S) are labeled.

[1] C. Wintgens EE Times (2009) The 50-nm DRAM battle rages on: An overview of Micron's technology  
[2] Y. Choi EE Times (2008) Under the Hood: Next steps in NAND Flash evolution  
[3] L. C. Tran IEEE (2004) Challenges of DRAM and Flash Scaling – Potentials in Advanced Emerging Memory Device

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