Charge Trapping Effects in High-k Transistors

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Note, this is not a real abstract but a template based from the real one. Transition metal and rare-earth oxides comprise many of the high dielectric constant (high-k) materials currently being investigated for application as gate dielectrics in highly scaled transistors. A common electronic feature of these materials is the presence of d-shell states, which leads to their structural properties being drastically different from those of the conventional SiO_2 gate dielectric [1, 2]. One of the high-k dielectric properties with significant implications for their electrical characteristics is a relatively high density of as-grown defects, which may function as electron traps and fixed charges. The latter can complicate the setting of symmetrical threshold voltage (V_t) values in N and P types devices, while diffusion of these charges at elevated temperature/voltage bias, as well as electron trapping/de-trapping in structural defects may contribute to threshold voltage instability and mobility degradation in transistors with the high-k gate stack. Understanding the kinetics of the charge trapping can provide helpful insight into the nature of the defects and ways to mitigate their adverse effects on device performance.

Indeed, ab initio DFT calculations have shown that the 4-coordinated O vacancy in the monoclinic HfO_2 results in the formation of a shallow, diffused electron trap state in the gap [8]. Location of the O vacancies in the polycrystalline dielectric – grain's bulk or boundaries – is still an open issue, although the temperature dependence of the O-K edge EELS spectra of the ALD HfO_2 film indicates that the density of the oxygen defects does not scale with the density of the grain boundaries [9]. Another potential candidate for the electron trap active in transient charging is Zr impurities usually present in hafnia at the level of few atomic percent. Substitutional Zr atoms generate shallow states at an energy level about 0.1 eV below the band edge, which are delocalized over an area well above 1 nm in diameter [8].

Charge trapping phenomena exhibit a strong dependence on the gate stack physical characteristics: in particular, high-k film composition, thickness, crystallinity, etc. - this is the subject of discussion in this work.

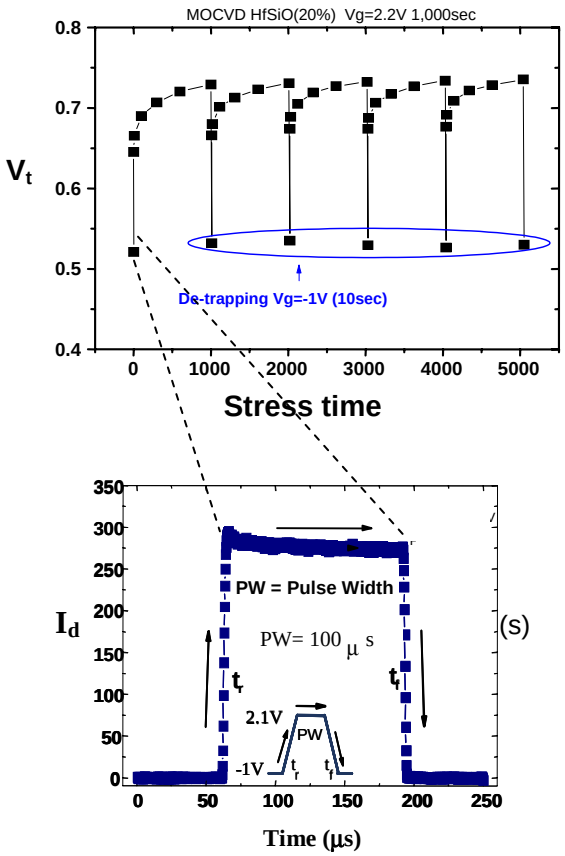

Fig. 1 (a) Variation of the NMOS transistor threshold voltage during stress cycles, which include 1000 sec substrate injection stress followed by 10 sec stress of the opposite bias under the specified voltage conditions. (b) The drain current change (μA) during the pulse, which approximately corresponds to the initial 100 μsec of

[1] G. Bersuker et al., Materials Today, p.26, Jan, 2004
[2] J. Lucovsky, IEEE TDMR, March, 2005
[3] J. H. Sim et al., SSDM, 214, 2004
[4] H. R. Harris et al., IRPS, 2005
[5] G. Bersuker et al., APL, 2005
[6] G. Ribes et al., IEEE-IRW, p. 125, 2004
[7] G. Bersuker et al., Mat.Res.Soc.Symp.Proc., 811, p. 31, 2004

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